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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,692	KUMAR ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on June 7, 2004

2. This application has been examined. Claims 1-39 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McCrory et al. (US No. 6,640,289) in view of Baumgartner et al. (US No. 6,344,177).

In regard to claim 1, McCrory et al. disclose a container object (i.e. software) stored in platform readable medium executed by a processor within a platform, (see col. 3, line 17 through col. 4, line 20); and a plurality of component objects to identify constituent components of the node (see col. 3 line 17 through col. 4, line 20). But McCrory et al. do not specifically disclose the hardware identification object to identify to an operating system of the platform that a type of device represented by the container object is a node. However Baumgartner et al. disclose the software partition to identify to an operating system of the platform that a type of device represented by the container object is a node (see col. 3, line 35 through col. 4, line 57). Therefore, it would have been obvious to a person of

an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 2, McCrory et al. disclose wherein the node is a scalability node controller 32 (i.e. SNC) (see figure 1).

In regard to claim 3, Baumgartner et al. disclose wherein the container object handles an ejection notice for a hot-plug removal of the scalability node controller and at least one component coupled the scalability node controller from the platform (see figure 4, col. 5, lines 42-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 4, McCrory et al. disclose wherein the at least one component includes a processor (see figure 1, col. 3, lines 17-27).

In regard to claim 5, McCrory et al. disclose wherein the at least one component includes a memory (see figure 1, col. 3, lines 17-27).

In regard to claim 6, Baumgartner et al. disclose wherein the ejection notice is provided by an operating system of the platform (see figure 4, col. 5, lines 42-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an

improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 7, Baumgartner et al. disclose wherein one of the plurality of component objects includes a processor object to identify one or more processors coupled to the node (see col. 3, line 35 through col. 4, line 57). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 8, Baumgartner et al. disclose wherein one of the plurality of component objects includes a device object to identify one or more memory devices coupled to the node (see col. 3, line 35 through col. 4, line 57). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 9, Baumgartner et al. disclose wherein any hot plug operation is applied as a single operation to the container object and its constituent objects (see figure 4, col. 5, lines 42-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 10, Baumgartner et al. disclose wherein hot plug addition of the one or more processors and the one or more memory devices belonging to the container object is notified to the operating system simultaneously in a single operation (see figure 4, col. 5, lines 42-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 11, Baumgartner et al. disclose wherein the hot plug removal of the processors and the memory devices belonging to the container object is notified to the operating system simultaneously in a single operation (see figure 4, col. 5, lines 42-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 12, Baumgartner et al. disclose wherein the container object handles a hot-plug addition by activating the memory devices associated with the device object online prior to activating the processors associated with the processor object (see figure 4, col. 5, lines 42-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for

supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 13, Baumgartner et al. disclose further comprising a proximity object to describe a proximity domain within the platform that the node belongs to (see col. 3, line 35 through col. 4, line 57). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

In regard to claim 14, Baumgartner et al. disclose wherein the proximity object is an assigned integer value to represent the proximity domain that the node belongs to (see col. 3, line 35 through col. 4, line 57). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Baumgartner et al. within the system of McCrory et al. because it would provide an improved method and system for supporting software partition and dynamic reconfiguration within a NUMA multiprocessor system.

5. Claims 15-39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McCrory et al. (US No. 6,640,289) in view of Dove et al. (US No. 5,938,765).

In regard to claims 15, 28, 34, 37, McCrory et al. disclose a system comprising: a memory device to store a system Basic Input/Output System (BIOS) (see col. 3, line 17 through col. 4, line 20); and a plurality of processor substrates in communication with the memory device, the plurality of processor substrates

including a first processor substrate including a first plurality of components (see col. 3, line 17 through col. 4, line 20), and a second processor substrate including a second plurality of components (see col. 3, line 17 through col. 4, line 20). But McCrory et al. do not specifically disclose each of the processor substrate containing a BIOS to initialize the plurality of components in response to hot-plug addition of the processor substrate. However Dove et al. disclose the multinode system utilizes the standard BIOS in each node to initialize the plurality of component within the node (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dove et al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claim 16, McCrory et al. disclose wherein the first plurality of components of the first processor substrate include a processor cluster and a memory cluster (see figure 1).

In regard to claim 17 McCrory et al. disclose wherein the first plurality of components of the first processor substrate further include a scalability node controller 32 coupled to the processor cluster and the memory cluster (see figure 1).

In regard to claim 18, McCrory et al. disclose wherein the scalability node controller of the first plurality of components is coupled to local memory of the memory cluster through a plurality of communication sub-links (see figure 1, col. 3, line3, line 17 through col. 4, line 20). But McCrory et al. do not specifically disclose the communication sub-links supporting a total data throughput of at least one Gigabyte per second. However one skilled in the art would have understood

that they can choose to implement the high-speed data transfer cards to provide fast data throughoutput.

In regard to claim 19, McCrory et al. disclose wherein the scalability node controller of the first plurality of components includes a plurality of scalability port interfaces coupled to a first connector of the first processor substrate (see figure 1, col. 3, line3, line 17 through col. 4, line 20).

In regard to claim 20, McCrory et al. disclose wherein the second plurality of components of the second processor substrate further include a secondary scalability node controller including a plurality of scalability port interfaces coupled to a second connector of the second processor substrate (see figure 1, col. 3, line 3, line 17 through col. 4, line 20).

In regard to claims 21, 29, McCrory et al. disclose further comprising: an interconnect substrate 50 including a third connector, a fourth connector and a fifth connector, the third connector adapted to mate with the first connector of the first processor substrate and coupled to the fifth connector via a first link and a second link, the fourth connector adapted to mate with the second connector of the second processor substrate and coupled to the fifth connector via a third link and a fourth link (see figure 1, col. 3, line 3, line 17 through col. 4, line 20).

In regard to claims 22, 30, McCrory et al. disclose further comprising: an input/output (I/O) substrate 62 including a sixth connector coupled to the fifth connector, the I/O substrate further includes (1) a first scalability port switch coupled to the first link and the third link, (2) a second scalability port switch coupled to the second link and the fourth link, (3) a first Server Input/Output Hub coupled to the first and second scalability port switches, and (4) a second Server

Input/Output Hub coupled to the first and second scalability port switches (see figure 1, col. 3, line 3, line 17 through col. 4, line 20).

In regard to claims 23, 31, 38, Dove et al. disclose wherein the first initialization BIOS contained in the first storage device, when executed, also establishes a communication path between the scalability node controller and at least one of the first scalability port switch and the second scalability port switch (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dove et al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claims 24, 32, Dove et al. disclose wherein the second initialization BIOS contained in the second storage device, when executed, also establishes a communication path between the secondary scalability node controller and at least one of the first scalability port switch and the second scalability port (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dove et al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claims 25, 33, Dove et al. disclose wherein the first initialization BIOS contained in the first storage device elects a processor from a plurality of processors associated with the processor cluster to act as a node boot strap processor for the first processor substrate (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at

the time the invention was made to have combined the teachings of Dove et al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claim 26, Dove et al. disclose wherein the second initialization BIOS contained in the second storage device elects a processor from a plurality of processors implemented on the second processor substrate to act as a node boot strap processor for the second processor substrate (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dove et al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claim 27, Dove et al. disclose wherein the first initialization BIOS contained in the first storage device initializing the first plurality of components prior to notification of an operating system running on the platform of the initialized hot-plugged first processor substrate (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dove et al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claim 35, Dove et al. disclose wherein the second platform is able to run an updated software application independent of and without interrupting operations of the first platform (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dove et

al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claim 36, Dove et al. disclose wherein the updated software application is an updated operating system (see col. 6, line 6 through col. 7, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dove et al. within the system of McCrory et al. to provide a highly reliable system since each node runs its own initialization independently.

In regard to claim 39, McCrory et al. disclose wherein the components on the first processor substrate include at least two processors (see figure 1).

Response to Amendment

6. Applicant's arguments, see pages 13-15, filed on June 7, 2004, with respect to the rejections of claims 15-39 under 35USC103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Dove.

Conclusion

7. All claims are rejected.

8. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Bouchier et al. (US No. 6,684,343) disclose a managing operations of a computer system having a plurality of partitions.

Talbot et al. (US No. 6,516,373) disclose a common motherboard interface for processor modules of multiple architectures.

Chu (US No. 6,718,415) discloses a computer system and method including console housing multiple computer modules having independent processing units, mass storage devices, and graphics controllers.

Gentile (US Pub No. 2002/0147941) discloses a network based BIOS receovery method

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
9/1/04